IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

C.A.T. SALAMA et al.

Serial No.: 10/617,487 Group Art Unit:2811

Filed: July 11, 2003 Examiner:

For: SUPER JUNCTION / RESURF LDMOST (SJR-LDMOST)

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Marc A. Rossi

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
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Sir:

Pursuant to 37 C.F.R. §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached Form PTO-1449. Copies of the references listed on Form PTO-1449 are attached.

It is respectfully requested that the information be expressly considered during the prosecution of this application, that these references be made of record therein and appear among the "References Cited" on any patent to issue therefrom, and that an initialed copy of the PTO-1449 be returned to the undersigned.

Respectfully submitted,

Date: 02/02/04

_____

Marc A. Rossi
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Attorney Docket No.: SALA:003

Sheet 1 of 1

INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

Docket Number (Optional) SALA:003	SERIAL NO.: 10/617,487
APPLICANT(s) SALAMA et al.	
FILING DATE: July 11, 2003	Group Art Unit 2811

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	US	4,754,310	6/88	Coe	357	13	
	US	5,216,275	6/93	Chen	257	493	
	US	5,438,215	8/95	Tihanyi	257	401	
	US	2003/0190789	10/03	Salama et al.	438	286	

OTHER DOCUMENT(S) (Including Author, Title, Date, Pertinent Pages, Etc.)

			"High Voltage Thin Layer Devices (Resurf Devices)"; J.A. APPELS et al.; IEEE International Electron Device Meeting (IEDM); Dig. Tech Papers; pp. 238-241; 1979.
			"Theory of a novel voltage-sustaining layer for power devices"; X.B. CHEN et al.; Microelectronics Journal, Vol. 29; pp. 1005-1011; 1998.
			"COOLMOS™ - a new milestone in high voltage Power MOS"; L. LORENZ et al.; Proceedings of the 11th International Symposium on Power Semiconductor Devices and ICs (ISPSD); pp. 3-10; 1999.
			"Super Junction LDMOST in Silicon-On-Sapphire Technology (SJ-LDMOST); Sameh NASSIF-KHALIL et al.; International Symposium on Power Semiconductor Devices and ICs (ISPSD), Proceedings; pp. 81-84; 2002.
			"170V Super Junction - LDMOST in a 0.5 μm Commercial CMOS/SOS Technology"; S.G. NASSIF-KHALIL et al.; International Symposium on Power Semiconductor Devices and ICs (ISPSD), Proceedings, accepted for publication; 4 pages.
			"Extended (180V) Voltage in 0.6 μm Thin-Layer-SOI A-BCD3 Technology on 1 μm BOX for Display, Automotive & Consumer Applications"; A.W. LUDIKHUIZE et al.; International Symposium on Power Semiconductor Devices and ICs (ISPSD), Proceedings; pp.77-80; 2002.
			"A Versatile 700-1200-V IC Process for Analog and Switching Applications"; Adriaan LUDIKHUIZE; IEEE Transactions on Electron Devices, vol. 38; pp. 1582-1589; 1991.
			"Experimental Results and Simulation Analysis of 250V Super Trench Power MOSFET (STM); T. NITTA et al.; International Symposium on Power Semiconductor Devices and ICs (ISPSD), Proceedings; pp. 77-80; 2000.
			"Super-Junction LDMOST on a Silicon-on-Sapphire Substrate"; S. NASSIF-KHALIL et al.; IEEE Transactions on Electron Devices, Vol. 50, No. 5; May 2003; pp. 1385-1391.
EXAMINER			DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.